US-PAT-NO: 4914746

DOCUMENT-IDENTIFIER: US 4914746 A

TITLE: Electronic digital still camera for separately storing component video signals in memory

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Abstract Text - ABTX (1):

A digital electronic still camera to which detachably connected is a semiconductor memory module adapted for storage of video signals representing a still image in the form of digital data. The camera includes a connector for detachably and electrically connecting the semiconductor memory module, an imaging subsystem including an image pickup device and adapted for imaging a scene and producing video signals representative of the scene in a dot-sequential manner, a signal processor for converting the video signals produced from the imaging device into component signals and developing the component signals in the form of digital signals, and a control unit for controlling the imaging subsystem and the signal processor to cause the imaging subsystem to shoot the scene, the control unit causing the signal processor to convert the resulting video signals into the component video signals. The control unit supplies control signals to the connector for writing the component signals into the semiconductor memory module.

Application Filing Date - AD (1):

19880429

TITLE - TI (1):

Electronic digital still camera for separately storing component video signals in memory

Brief Summary Text - BSTX (6):

The solid state imaging devices mounted on the camera, in general, have an array of color filter segments and spectral transmittivities that are proper to the specific imaging devices. Thus, various combinations of pixels are employed, such as the combinations of pixels of cyan (Cy), magenta (M), yellow (Ye) and green (G); red (R), green (G) and blue (B); or cyan (Cy), white (W), yellow (Ye) and green (G). In certain imaging devices, the pixels in a line are different in color from pixel to pixel, while in others, the pixels of the same color are arrayed in the perpendicular direction of a screen.

Detailed Description Text - DETX (11):

As shown for example in FIG. 9, the signal processing circuit 40 preferably includes a color separator circuit 100, a white balance adjustment circuit 102 and a gamma corrector 104. To the color separator circuit 100 is connected a signal input 38. The color separator 100 operates to separate pixel-sequential video signals at the input 38 into color-separated component signals, such as red (R), green (G) and blue (B) signals, in accordance with pixel clocks received from the control circuit 24 over the control line 50. This color separation is carried out in accordance with the array of the filter segments of the color filter 28 of the image pickup device 22. The filter segments may be arrayed in any suitable manner.

Detailed Description Text - DETX (13):

FIG. 10 shows an alternative embodiment of the signal processing circuit 40. The signal processing circuit 40 differs from the embodiment shown in FIG. 9 in that a matrix 106 is arranged between the output 42 and the output of the gamma corrector 104 in the embodiment of FIG. 10. The matrix 106 operates to produce a luminance signal Y and chrominance or color-difference signals R-Y and B-Y from the component signals R, G and B obtained at the gamma corrector 104 to transmit these luminance and color-difference signals at the three outputs 42. In this manner, the luminance signal Y and color-difference signals R-Y are issued to the outputs 42 of the signal processing circuit 40.

Detailed Description Text - DETX (16):

The control circuit 24 enables the analog-to-digital converter 36 and the signal processing circuit 40 in response to sync signals produced by the sync generator 30. Thus the dot-sequential video signals are converted by the analog to digital converter 36 into corresponding digital data before being fed to the signal processing circuit 40. In the circuit 40 the digital data are separated in the color separating circuit 100 into for example three color component signals of red (R), green (G) and

blue (**B**). The resulting three component signals are then adjusted for white balance and gradation in the white balance adjustment circuit 102 and the gamma corrector circuit 104, respectively. The video signals, thus modified in various manners, are issued at the output 42 in the form of the color signals **R, G and B** or the data of the luminance signal Y and the color-difference signals **R**-Y and **B**-Y, in the form of component signal data.

Detailed Description Text - DETX (19):

In the present embodiment, the video signals stored in the memory 90 in the form of, for example, **R, G and B** component signals, may be reproduced by a playback unit 120 shown for example in FIG. 11. The playback unit 120 has a connector 122 to which the memory 90 is detachably connected and by means of which a read-out data line 96 of the memory 90 is connected through a digital-to-analog converter or DAC 124 to a matrix 126. The memory 90 also has its control line 94 connected through connector 122 to a control circuit 128.

Detailed Description Text - DETX (20):

The **component video** signal data **R, G and B** read-out on the **output** data line 96 of the memory 90 may be converted by DACs 124 into corresponding analog signals which are then converted by the matrix 126 into the luminance signals Y and color-difference signals **R**-Y and **B**-Y. These signals are then introduced into an encoder 130 where they are converted into **composite video** signals which are then issued at the **output** 132. To this **output** connected is a **video output** device such as a **video** monitor 134 and/or a printer by means of which the **composite video** signals at the **output** 132 are visualized in the form of the visible image.

Detailed Description Text - DETX (21):

The various elements of the playback unit 120 are controlled by the control circuit 128. The control circuit 128 is responsive to operator's commands entered at the operation and display unit 136 to supply control signals for read-out thereof on the control line 94 of the memory 90 in accordance with a predetermined basic frequency, whereby the video signal data for a specified picture image are read out from the memory 90. These **video** signal data take the form of component signals, herein color signals of **R, G and B,** so that they are converted by a **video** signal processing circuit consisting of the matrix 126 and the encoder 130 into **composite video** signals which are then issued at the **output** 132. In this manner, the image represented by the video signals are visually displayed on the image monitor 134.

Detailed Description Text - DETX (22):

FIG. 2 shows an alternative embodiment of the digital electronic still camera which differs from the embodiment of FIG. 1 in that a switching circuit 56 is connected to three output lines 42 of the signal processing circuit 40 and has its output 58 connected to the data line of the connector 14. In the following description, the parts or elements similar to those shown in FIG. 1 are denoted by the same reference numerals. The switching circuit 56 is a selective circuit that may take either one of three selective connecting positions responsive to a control output 60 of the control circuit 24. The control circuit 24 issues switching signals associated with pixel clocks to the control line 60. Thus, the switching circuit 56 causes the color-separated component signals **R, G and B** or the luminance signal Y and the color-difference signals **R**-Y and **B**-Y at the three outputs 42 of the signal processing circuit 40, that is, the component signal data, to be issued dot- or pixel-sequentially at the output 58. These signal data are transmitted through the connector 14 and the data line 92 of the memory 90 so as to be written therein as the dot- or pixel-sequential video signal data.

Detailed Description Text - DETX (23):

FIG. 3 shows a further alternative embodiment which differs from the embodiment of FIG. 2 in that the video signal output 38 of the image pickup device 22 is directly connected to the input 38 of the signal processing circuit 40 and that three analog-to-digital converters 62 are connected between the three outputs 42 of the circuit 40 and the switching circuit 56. Thus the signal processing circuit 40 is of the circuit configuration in which the video signals produced by the image pickup device 22 are processed while they remain in the form of analog signals. Similarly to the analog to digital converter 36, the analog to digital converters 62 operate to convert the analog format **component video** signals at the input 42 into corresponding digital data of, for example, eight bits, before the signals are issued at the **output** 64.

Detailed Description Text - DETX (24):

FIG. 4 shows another embodiment of the present invention wherein a single circuit analog-to-digital converter 68 is provided at the output side of the switching circuit 56 in place of the three-circuit type analog-to-digital converters 62. The present embodiment differs from the embodiment of FIG. 3 in that the switching circuit 56 is connected to the three outputs 42 of the signal processing circuit 40 and has its output 58 connected to a data line 70 of the connector 14 through the analog-to-digital

converter 68. Therefore, the signal processing circuit 40 also has a circuit configuration in which the output video signals from the image pickup device 22 are processed while they remain in the form of analog signals. The analog-to-digital converter 68 operates to convert the dot-sequential **component video** signals of the analog format at the **output** 58 into corresponding digital data before the signals are issued at the **output** 70. In a manner different from the embodiment shown in FIG. 3, only one circuit of the analog to digital converter 68 is necessary herein such that the overall system may be simplified in structure.

Detailed Description Text - DETX (26):

The video signals thus written in the memory 90 as the line-sequential chrominance signals are reproduced by the playback unit 120 shown for example in FIG. 12. The FIG. 12 playback circuit 120 differs from the circuit configuration of FIG. 11 in that it has a sequential-line concurrent-combining circuit 138 for concurrently combining the color-difference signals R-Y and B-Y read out line-sequentially from the memory 0, while it does not have the matrix 126. The data of the color-difference signals R-Y and B-Y read out line-sequentially from the memory 90 are converted by the digital-to-analog converters 124 into corresponding analog signals while the chrominance signals of the lacking scanning lines are interpolated and concurrently combined with those of the existing scanning lines. The **composite video** signals are formed in the encoder 30 using these combined chrominance signals and the luminance signal Y so as to be issued at the **output** 132.

EXAMINER'S SEARCH NOTES

United States Patent [19]

Nishi et al.

[11] **Patent Number: 4,914,746**

[45] **Date of Patent: Apr. 3, 1990**

[54] **ELECTRONIC DIGITAL STILL CAMERA FOR SEPARATELY STORING COMPONENT VIDEO SIGNALS IN MEMORY**

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[73] Assignee: **Fuji Photo Film Co., Ltd., Kanagawa, Japan**

[21] Appl. No.: **188,403**

[22] Filed: **Apr. 29, 1988**

[30] **Foreign Application Priority Data**

May 1, 1987 [JP] Japan 62-106239

[51] **Int. Cl.⁴** **H04N 3/14; H04N 5/76**

[52] **U.S. Cl.** **358/334**; 358/906; 358/909; 358/44

[58] **Field of Search** 358/41, 43, 44, 909, 358/906, 310, 334, 335

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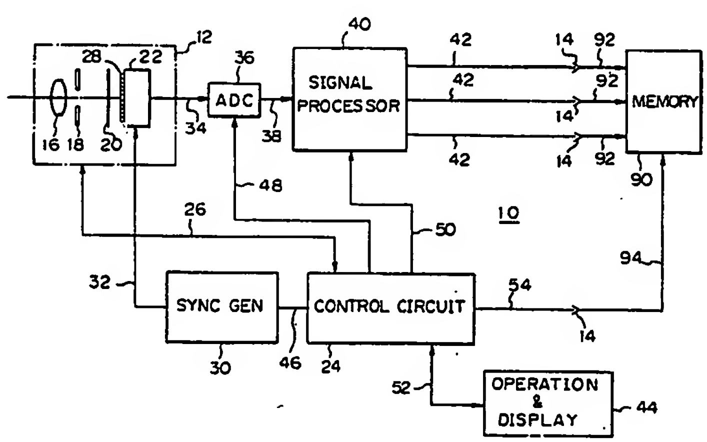
Assistant Examiner—Mark R. Powell
Attorney, Agent, or Firm—Birch, Stewart, Kolasch & Birch

[57] **ABSTRACT**

A digital electronic still camera to which detachably connected is a semiconductor memory module adapted for storage of video signals representing a still image in the form of digital data. The camera includes a connector for detachably and electrically connecting the semiconductor memory module, an imaging subsystem including an image pickup device and adapted for imaging a scene and producing video signals representative of the scene in a dot-sequential manner, a signal processor for converting the video signals produced from the imaging device into component signals and developing the component signals in the form of digital signals, and a control unit for controlling the imaging subsystem and the signal processor to cause the imaging subsystem to shoot the scene, the control unit causing the signal processor to convert the resulting video signals into the component video signals. The control unit supplies control signals to the connector for writing the component signals into the semiconductor memory module.

11 Claims, 12 Drawing Sheets



US-PAT-NO: 6278492

DOCUMENT-IDENTIFIER: US 6278492 B1

TITLE: Method and apparatus for transmitting digital color signals to a camera

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Abstract Text - ABTX (1):

A method and apparatus for transmitting digital color imaging signals to a camera controlling unit at a pre-set sampling rate obtained on imaging using a CCD imaging device. The sampling rate of at least one of plural signal components making up the digital color imaging signals is converted so that the sampling rate will be higher than the pre-set sampling rate. The digital color imaging signals containing at least one signal component having the converted sampling rate are transmitted to the camera control unit.

Application Filing Date - AD (1):

19970221

TITLE - TI (1):

Method and apparatus for transmitting digital color signals to a camera

Brief Summary Text - BSTX (8):

Referring to FIG. 1, the light from an object, incident on a lens system 201 of a camera head 200, is separated by a color separation prism 202 into light beams of three colors, namely red (R), green (G) and blue (B). The light beams of R, G and B are incident on solid-state imaging devices (CCDs) 203a, 203b and 203c for conversion into electrical signals corresponding to the R, G and B colors, respectively. For exploiting the technique of the pixel offsetting technique, the CCDs 203R, 203G and 203B are arranged so that the CCD 203R and the CCD 203B are horizontally offset relative to the CCD 203G by one-half the pixel pitch. Consequently, the image incident on the CCDs 203R, 203G and 203B has imaging signals for G complementally sampled with respect to the imaging signals for R and B.

Brief Summary Text - BSTX (9):

The imaging signals for R, G and B from the CCDs 203R, 203G and 203B are amplified by associated pre-amplifiers 204R, 204G and 204B, respectively, so as to be then converted by analog/digital (A/D) converters 205R, 205G and 205B, respectively, into digital imaging signals. It is noted that the A/D converters 205R, 205G and 205B convert analog imaging signals into digital signals using clocks of the same frequency as the sampling clocks used in the CCDs 203R, 203G and 203B, while the A/D converter 205G for G perform digital conversion with clocks delayed in phase by 180.degree. from those used in the A/D converters 205R and 205B for R and B, respectively, for realizing the pixel offsetting effect. In the example of FIG. 1, the frequency of the digital imaging signals outputted by the (A/D) converters 205R, 205G and 205B is 18 MHz.

Brief Summary Text - BSTX (12):

The R, G and B component signals, rate-converted by the frequency conversion circuit 207, are converted by a parallel/serial conversion circuit (P/S conversion circuit) 208 into composite signals of the above-mentioned SMPTE 295M standard so as to be outputted along with various other sorts of the information at an output terminal 209.

Brief Summary Text - BSTX (14):

The composite digital imaging signals, supplied to the camera control unit 210, are converted by a serial/parallel conversion circuit (S/P conversion circuit) 212 into component digital imaging signals of R, G and B. These component digital imaging signals of R, G and B are converted into analog imaging signals by digital/analog (D/A) converting circuits 213R, 213G and 213B associated with R, G and B, respectively, so as to be outputted at output terminals 214R, 214G and 214B, similarly associated with R, G and B, respectively.

Brief Summary Text - BSTX (15):

If the **composite** digital **video** signals of the above-mentioned SMPTE 295M standard are outputted by the camera control unit 210, the **R, G and B** component digital **video** signals from the S/P conversion circuit 212 are converted by the P/S conversion circuit 216 into **composite** signals of the above-mentioned SMPTE 295M standard which are outputted at an **output** terminal 217. Meanwhile, if the rate of the component digital video signals of **R, G and B** from the S/P conversion circuit 212 S, for example, 18 MHz, it is converted by a frequency converter 215 into the rate of 13.5 MHz and thence supplied to the P/S conversion circuit 216.

Detailed Description Text - DETX (4):

Referring to FIG. 2, the light from an object, incident on a lens system 11 of a camera head 10, is sent to a color-separation prism 12. The lens system 11 includes, in addition to a lens for imaging the light from the object on a CCD, a light stop unit for light volume adjustment or setting the depth of field and a lens driving mechanism for focusing. The lens system 11 may additionally include an IR cut filter or a UV cut filter, if so desired. The color-separation filter 12 is comprised of, for example, a dichroic prism, and separates the incident light on the lens 11 into red (**R**), green (**G**) and blue (**B**) beams, which are conducted towards CCDs 13R, 13G and 13B for **R, G and B,** respectively.

Detailed Description Text - DETX (5):

These **R, G and B** light beams are converted by the associated CCDs 13R, 13G and 13B into imaging signals associated with **R, G and B,** respectively. In the camera head 10 shown in FIG. 2, the CCDs 13R, 13G and 13B are arranged so that the CCDs 13R and 13B for **R and B** are horizontally offset by one-half the pixel pitch with respect to the CCD 13G for **G.** Consequently, the images incident on the CCDs 13R, 13G and 13B have the imaging signals for **G** complementally sampled with respect to the imaging signals for **R and B.**

Detailed Description Text - DETX (6):

The imaging signals for **R, G and B** from the CCDs 13R, 13G and 13B are amplified by associated pre-amplifiers 14R, 14G and 14B, respectively, and subsequently converted into digital imaging signals by analog/digital (A/D) conversion circuits 15R, 15G and 15B, respectively. The A/D conversion circuits 15R, 15G and 15B digitally convert the analog imaging signals, using the clocks of the same frequency as that of the sampling clocks in the CCDs 13R, 13G and 13B. In the A/D conversion circuit 15G for G, digital conversion is performed with clocks delayed in phase by 180.degree. from the A/D conversion circuits 15R and 15B for producing the pixel offsetting effect. In the embodiment of FIG. 2, the frequency of the digital imaging signals outputted by the A/D conversion circuits 15R, 15G and 15B is 18 MHz.

Detailed Description Text - DETX (8):

The above-mentioned **R, G and B** component digital **video** signals, obtained by the digital processing circuit 16, are converted by a P/S conversion circuit 17 into serial **composite** digital **video** signals which are outputted along with various other sorts of the information at an **output** terminal 18. Although no particular reference is made to the format of the serial digital video signals outputted at the output terminal 18, compatibility in format is maintained between the camera head 10 and the camera control unit.

Detailed Description Text - DETX (10):

The serial digital video signals of **R, G and B,** supplied to the camera control unit 20, are converted by an S/P conversion circuit 22 into **R, G and B** component digital video signals. These digital video signals of **R, G and B** are converted by D/A conversion circuits 23R, 23G and 23B associated with **R, G and B,** respectively, into analog video signals, which are outputted at output terminals 24R, 24G and 24B similarly associated with **R, G and B,** respectively.

Detailed Description Text - DETX (11):

When the above-mentioned SMPTE 295M standard composite digital video signals are outputted from the camera control unit 20, the **R, G and B** component digital video signals from the S/P conversion circuit 22 are converted by a frequency conversion circuit 25 to a rate of, for example, 13.5 MHz, before being sent to a P/S conversion circuit 26. The digital **video** signals, converted by the P/S conversion circuit 26 into the SMPTE 295M standard **composite** digital **video** signals, are outputted at an **output** terminal 27.

Detailed Description Text - DETX (12):

In the above-described first embodiment, the limit resolution obtained from the 36 MHz rate digital video signals obtained with the digital processing circuit 206 of the camera head 200 is ideally approximately 1400. This rate is maintained when the digital video signals are transmitted to the camera control unit 20. Therefore, the **R, G and B** component digital video signals outputted at the output terminals 24R, 24G and 24B of the camera control unit 20 are of the above-mentioned resolution. That is, since the digital video signals are transmitted to the camera control unit 20 in the present first embodiment at a rate twice the CCD sampling clocks, it becomes possible to output video signals of high resolution obtained by pixel offsetting from the camera control unit 20. For taking advantage of the effect of the pixel offsetting in the camera head on improving the resolution, it suffices if the frequency of the camera head output is set so as to be higher than the CCD sampling frequency, as in the first embodiment described above. However, for simplifying the processing, it is desirable to set the rate of the video signals outputted by the camera head so as to assure facilitated conversion by the camera control unit. For example, if the camera control unit **outputs** the SMPTE 295M standard **composite** digital **video** signals with the frequency of 13.5 MHz, it is desirable that the rate of the **video** signals outputted by the camera head be an integer number of times 13.5 MHz obtained on conversion by the camera control unit. Specifically, with the sampling frequency of the CCD of the camera head of 18 MHz, the rate of the video signals outputted by the camera head is desirably higher than 18 MHz and equal to an integer number times, such as two times of 13.5 MHz, or 27 MHz.

Detailed Description Text - DETX (14):

Referring to FIG. 3, the light from an object, incident on the lens system 31 of the camera head 30, is separated by a color-separating prism 32 into **R, G and B** beams, which are conducted towards a CCD 33R for **R,** a CCD 33G for **G** and a CCD 33B for **B,** respectively. These **R, G and B** beams are converted by the associated CCD 33R, CCD 33G and CCD 33B into imaging beams associated with **R, G and B,** respectively, and amplified by associated pre-amplifiers 34R, 34G and 34B so as to be supplied to A/D converters 35R, 35G and 35B, respectively. The imaging signals, converted into digital signals by the A/D converters 35R, 35G and 35B, are processed by a digital processing circuit 36. The frequency of the digital imaging signals, obtained on processing by the digital processing circuit 36, is twice the frequency of the input digital imaging signals (18 MHz), or 36 MHz.

Detailed Description Text - DETX (15):

The above-mentioned **R, G and B** component digital signals, obtained by the digital processing circuit 36, are converted to the rate of 27 MHz by the frequency converter 37 and thence supplied to a P/S converter 38. The P/S converter 38 converts the **R, G and B** component digital signals from the frequency converter 37 into serial digital video signals which are then outputted along with other various sorts of the information at an output terminal 39. Although no particular reference is made to the format of the serial digital video signals outputted at the output terminal 39, compatibility in format is maintained between the camera head 30 and the camera control unit 40.

Detailed Description Text - DETX (17):

The serial digital video signals of **R, G and B,** supplied to the camera control unit 40, are converted by an S/P conversion circuit 42 into **R, G and B** component digital video signals. These digital video signals of **R, G and B** are converted by D/A conversion circuits 43R, 43G and 43B associated with **R, G and B,** respectively, into analog video signals, which are outputted at output terminals 44R, 44G and 44B similarly associated with **R, G and B,** respectively.

Detailed Description Text - DETX (18):

When the above-mentioned SMPTE 295M standard composite digital video signals are outputted from the camera control unit 40, the **R, G and B** component digital video signals from the S/P conversion circuit 42 are converted by a frequency conversion circuit 45 to a rate of, for example, 13.5 MHz, before being sent to a P/S conversion circuit 46. The digital **video** signals, converted by the P/S conversion circuit 46 into the SMPTE 295M standard **composite** digital **video** signals, are outputted at an **output** terminal 47.

Detailed Description Text - DETX (19):

In the above-described second embodiment, since the sampling rate of the digital video signals transmitted from the camera head 30 to the camera control unit 40 is 27 MHz, the **R, G and B component video** signals, outputted by **output** terminals 44R, 44G and 44B of the camera control unit 40, are of a limit resolution exceeding 1000. That is, it becomes similarly possible with the present second embodiment to output video signals of high resolution from the camera control unit 40. In addition, since the digital video signals of a rate that permits facilitated conversion by the camera control unit 40 are outputted by the camera head 30, rate conversion by the camera control unit 40 is facilitated.

Detailed Description Text - DETX (21):

If, in signal transmission between the camera head and the camera control unit, 10 bits each of the **R, G and B** digital signals are transmitted at a sampling rate of 27 MHz, the transmission channel of at least 810 Mbits/sec, inclusive of the signalless portion, is required in the absence of data compression. Thus, if a system in which the **R, G and B** digital signals of 10 bits each are transmitted at a sampling rate of 13.5 MHz and, in addition, the high-resolution luminance signals Y of 10 bits are transmitted at a sampling rate of 27 MHz/sec, a transmission channel of 675 Mbits/sec suffices for digital video signals in the signal transmission between the camera head and the camera control unit.

Detailed Description Text - DETX (23):

Referring to FIG. 4, the light from an object, incident on the lens system 51 of the camera head 50, is separated by a color-separating prism 52 into **R, G and B** beams, which are conducted towards a CCD 53R for **R,** a CCD 53G for **G** and a CCD 53B for **B,** respectively. These **R, G and B** beams are converted by the associated CCD 53R, CCD 53G and CCD 53B into imaging beams associated with **R, G and B,** respectively, and amplified by associated pre-amplifiers 54R, 54G and 54B so as to be supplied to A/D converters 55R, 55G and 55B, respectively. The imaging signals, converted into digital signals by the A/D converters 55R, 55G and 55B, are processed by a digital processing circuit 56. The frequency of the digital imaging signals, obtained on processing by the digital processing circuit 56, is twice the frequency of the input digital imaging signals (18 MHz), or 36 MHz.

Detailed Description Text - DETX (24):

The above-mentioned **R, G and B** component digital signals, obtained by the digital processing circuit 56, are sent to a matrix circuit 57. The matrix circuit 57 generates a digital luminance signal Y from the above-mentioned **R, G and B** digital signals and outputs the generated luminance signal. In addition, the matrix circuit 57 outputs the **R, G and B** digital signals. The signal rates of the digital luminance signal Y and the **R, G and B** digital signals are each 36 MHz.

Detailed Description Text - DETX (25):

The digital luminance signal Y and the **R, G and B** digital signals, outputted from the matrix circuit 57, are sent to a frequency conversion circuit 58. This frequency conversion circuit 58 converts the signal rate of the luminance signal Y and that of the **R, G and B** digital signals to 27 MHz and 13.5 MHz, respectively.

Detailed Description Text - DETX (26):

The signals converted in signal rate by the frequency conversion circuit 58 are sent to a P/S conversion circuit 59. The P/S conversion circuit 59 converts the digital luminance signal Y and the **R, G and B** digital signals into serial digital signals which are outputted at an output terminal 60 along with various other sorts of the information. Although no particular reference is made to the format of the serial digital video signals outputted at the output terminal 60, compatibility in format is maintained between the camera head 50 and the camera control unit 70.

Detailed Description Text - DETX (28):

The serial digital video signals of **R, G and B,** supplied to the camera control unit 70, are converted by an S/P conversion circuit 72 into **R, G and B** component digital video signals. Meanwhile, the signal rate of the digital luminance signal Y outputted by the S/P conversion circuit 72 is 27 MHz, while that of the digital video signals for **R, G and B** is 13.5 MHz. The digital luminance signal Y, having the signal rate of 27 MHz, is converted by a D/A converter 73Y into analog luminance signal which is outputted at an output terminal 74Y.

Detailed Description Text - DETX (29):

The digital video signals of **R, G and B** from the S/P conversion circuit 72 may be converted into analog signals and outputted from the camera control unit 70 as in the second embodiment described above. However, in the present third embodiment, digital color difference signals **R**-Y and **B**-Y are generated from the digital video signals of **R, G and B** from the S/P conversion circuit 72 and converted into analog signals, which are outputted.

Detailed Description Text - DETX (30):

The digital video signals for **R, G and B,** with the signal rate of 13.5 MHz, outputted by the S/P conversion circuit 72, are sent to a matrix circuit 75, which then generates the digital luminance signal Y and the digital color difference signals **R**-Y and **B**-Y from the digital video signals of **R, G and B** from the S/P conversion circuit 72 and outputs the generated color difference

signals. The signal rates of the digital luminance signal Y and the digital color difference signals R-Y and B-Y, formed by the matrix circuit 75, are each 13.5 MHz.

Detailed Description Text - DETX (35):

In the above-described third embodiment, the transmission channel may be diminished because the luminance signal Y and the digital signals for **R, G and B,** transmitted from the camera head 50 to the camera control unit 70, are transmitted at a rate of 27 MHz and at a rate of 13.5 MHz, respectively. Since the luminance signal Y is transmitted at the rate of 27 MHz, high-resolution video signals can be produced. Since the rate of the luminance signal Y transmitted from the camera head 50 is set at 27 MHz that can be converted easily by the camera control unit 70, rate conversion by the camera control unit 70 is facilitated.

Detailed Description Text - DETX (36):

If the luminance signal Y is transmitted from the camera head along with the **R, G and B** signals as in the above-described third embodiment, ii becomes possible for the camera head to perform on/off switching control of outputting of the luminance signal Y. By so doing, if the luminance signal Y is not needed or cannot be used by the camera control unit, the luminance signal Y may be designed so as not be transmitted from the camera head. On the other hand, if the luminance signal Y can be used or is needed by the camera control unit, the luminance signal Y can be transmitted from the camera head. This raises the interchangeability between the camera head and the camera control unit such that superfluous circuitry can be dispensed with if high resolution is not required.

Detailed Description Text - DETX (37):

In the above-described first to third embodiments, the **R, G and B** digital signals are transmitted between the camera head and the camera control unit. However, it is also possible to transmit the luminance signal Y and the color difference signals R-Y and B-Y, as in a fourth embodiment now explained by referring to FIG. 5.

Detailed Description Text - DETX (39):

Referring to FIG. 5, the light from an object, incident on the lens system 81 of the camera head 80, is separated by a color-separating prism 82 into **R, G and B** beams, which are conducted towards a CCD 83R for **R,** a CCD 83G for **G** and a CCD 83B for **B,** respectively. These **R, G and B** beams are converted by the associated CCD 83R, CCD 83G and CCD 83B into imaging beams associated with **R, G and B,** respectively, and amplified by associated pre-amplifiers 84R, 84G and 84B so as to be supplied to A/D converters 85R, 85G and 85B, respectively. The imaging signals, converted into digital signals by the A/D converters 85R, 85G and 85B, are processed by a digital processing circuit 86. The frequency of the digital imaging signals, obtained on processing by the digital processing circuit 86, is twice the frequency of the input digital imaging signals (18 MHz), or 36 MHz.

Detailed Description Text - DETX (40):

The above-mentioned **R, G and B** component digital signals, obtained by the digital processing circuit 86, are sent to a matrix circuit 87. The matrix circuit 87 generates a digital luminance signal Y and the color difference signals **R**-Y and **B**-Y from the above-mentioned **R, G and B** digital signals and outputs the signals. The signal rates of the digital luminance signal Y and the color difference signals R-Y and B-Y are each 36 MHz.

Detailed Description Text - DETX (52):

Referring to FIG. 6, the light from an object, incident on the lens system 111 of the camera head 110, is separated by a color-separating prism 112 into **R, G and B** beams, which are conducted towards a CCD 113R for **R,** a CCD 113G for **G** and a CCD 113B for **B,** respectively. These **R, G and B** beams are converted by the associated CCD 113R, CCD 113G and CCD 113B into imaging beams associated with **R, G and B,** respectively, and amplified by associated pre-amplifiers 114R, 114G and 114B so as to be supplied to A/D converters 115R, 115G and 115B, respectively. The imaging signals, converted into digital signals by the A/D converters 115R, 115G and 115B, are processed by a digital processing circuit 116. The frequency of the digital imaging signals, obtained on processing by the digital processing circuit 116, is twice the frequency of the input digital imaging signals (18 MHz), or 36 MHz.

Detailed Description Text - DETX (53):

The above-mentioned **R, G and B** component digital signals, obtained by the digital processing circuit 116, are sent to a matrix circuit 117. The matrix circuit 117 generates a digital luminance signal Y and digital color difference signals **R**-Y and **B**-Y from the above-mentioned **R, G and B** digital signals, and outputs the generated signals. The signal rates of the digital luminance signal Y and the digital signals color difference signals R-Y and B-Y are each 36 MHz.

Detailed Description Text - DETX (66):

Referring to FIG. 7, the light from an object, incident on the lens system 141 of the camera head 140, is separated by a color-separating prism 142 into **R, G and B** beams, which are conducted towards a CCD 143R for **R,** a CCD 143G for **G** and a CCD 143B for **B,** respectively. The CCDs 143R, 143G and 143B are associated with the aspect ratio of 16:9. These **R, G and B** beams, color-separated by the color-separating prism 142, are converted by the associated CCD 143R, CCD 143G and CCD 143B into imaging beams associated with **R, G and B,** respectively, and amplified by associated pre-amplifiers 144R, 144G and 144B so as to be supplied to A/D converters 145R, 145G and 145B, respectively. The imaging signals, converted into digital signals by the A/D converters 145R, 145G and 145B, are processed by a digital processing circuit 146. The frequency of the digital imaging signals, obtained on processing by the digital processing circuit 146, is twice the frequency of the input digital imaging signals (18 MHz), or 36 MHz.

Detailed Description Text - DETX (67):

The **R, G and B** component digital video signals, obtained by the digital processing circuit 146, are sent to an aspect ratio conversion circuit 147. If the imaging signals with the aspect ratio of 16:9 are transmitted to the camera control unit 160, the aspect ratio conversion circuit 147 directly outputs the **R, G and B** component digital video signals supplied by the digital processing circuit 146 without performing the aspect ratio converting operation. If the imaging signals with the aspect ratio of 4:3 are transmitted to the camera control unit 160, the aspect ratio conversion circuit 147 converts the **R, G and B** digital signals matched to the aspect ratio of 16:9 into digital signals matched to the aspect ratio of 4:3. That is, the aspect ratio conversion circuit 147 slices image portions corresponding to the aspect ratio of 4:3 from imaging signals obtained from the CCDs 143R, 143G and 143B for the aspect ratio of 16:9 by way of performing aspect ratio conversion. Meanwhile, if the aspect ratio conversion is not performed by the aspect ratio conversion circuit 147, the aspect ratio conversion circuit 147 outputs **R, G and B** digital signals with the rate of 36 MHz. If the aspect ratio conversion is performed by the aspect ratio conversion circuit 147, the aspect ratio conversion circuit 147 outputs **R, G and B** digital signals with the rate equal to 3/4 times that for the aspect ratio of 16:9 or 27 MHz (equal to 3/4 times 2 or 3/2 of the sampling clocks for the CCD of 18 MHz).

Detailed Description Text - DETX (68):

The **R, G and B** digital signals, outputted by the aspect ratio conversion circuit 147, are sent to a frequency conversion circuit 148. This frequency conversion circuit 148 converts the 36 MHz rate to 27 MHz if the aspect ratio conversion is not performed by the aspect ratio conversion circuit 147. If the aspect ratio conversion is done by the aspect ratio conversion circuit 147, the frequency conversion circuit 148 directly outputs the 27 MHz rate signal from the aspect ratio conversion circuit 147. Thus the frequency conversion circuit 148 outputs the 27 MHz rate **R, G and B** signals.

Detailed Description Text - DETX (70):

The signals converted in signal rate by the frequency conversion circuit 148 are sent to a P/S conversion circuit 149. The P/S conversion circuit 149 converts the **R, G and B** component digital **video** signals into serial **composite** digital **video** signals which are outputted at an **output** terminal 150 along with various other sorts of the information. Although no particular reference is made to the format of the serial digital video signals outputted at the output terminal 150, compatibility in format is maintained between the camera head 140 and a camera control unit 160.

Detailed Description Text - DETX (71):

The **composite** digital **video** signals outputted at the **output** terminal 150 are sent via a cable or the like to an input terminal 161 of the camera control unit 160.

Detailed Description Text - DETX (72):

The composite digital video signals, supplied to the camera control unit 160, are converted by an S/P conversion circuit 162 into **R, G and B** component digital video signals. Meanwhile, the signal rate of the **R, G and B** component digital video signals outputted by the S/P conversion circuit 162 is 27 MHz.

Detailed Description Text - DETX (73):

The **R, G and B** component digital video signals from the S/P conversion circuit 162 are converted by D/A conversion circuits 163R, 163G and 163B provided in association with **R, G and B,** respectively, so as to be outputted at output terminals 164R, 164G and 164B associated with **R, G and B,** respectively.

Detailed Description Text - DETX (74):

If the **R, G and B** component digital video signals, for example, are outputted from the camera control unit 160, the **R, G and B** digital video signals from the S/P conversion circuit 162 are converted in signal transmission rate to 13.5 MHz by the frequency conversion circuit 165 to 13.5 MHz before being sent to a P/S conversion circuit 166. The digital video signals, thus converted by the P/S conversion circuit 166, are outputted at an output terminal 167.

EXAMINER'S NOTES

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Nakamura

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(45) **Date of Patent: *Aug. 21, 2001**

(54) **METHOD AND APPARATUS FOR TRANSMITTING DIGITAL COLOR SIGNALS TO A CAMERA**

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(73) Assignee: **Sony Corporation**, Tokyo (JP)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(52) **U.S. Cl.** **348/441**; 348/262
(58) **Field of Search** 348/262, 263, 348/264, 265, 441, 453, 488

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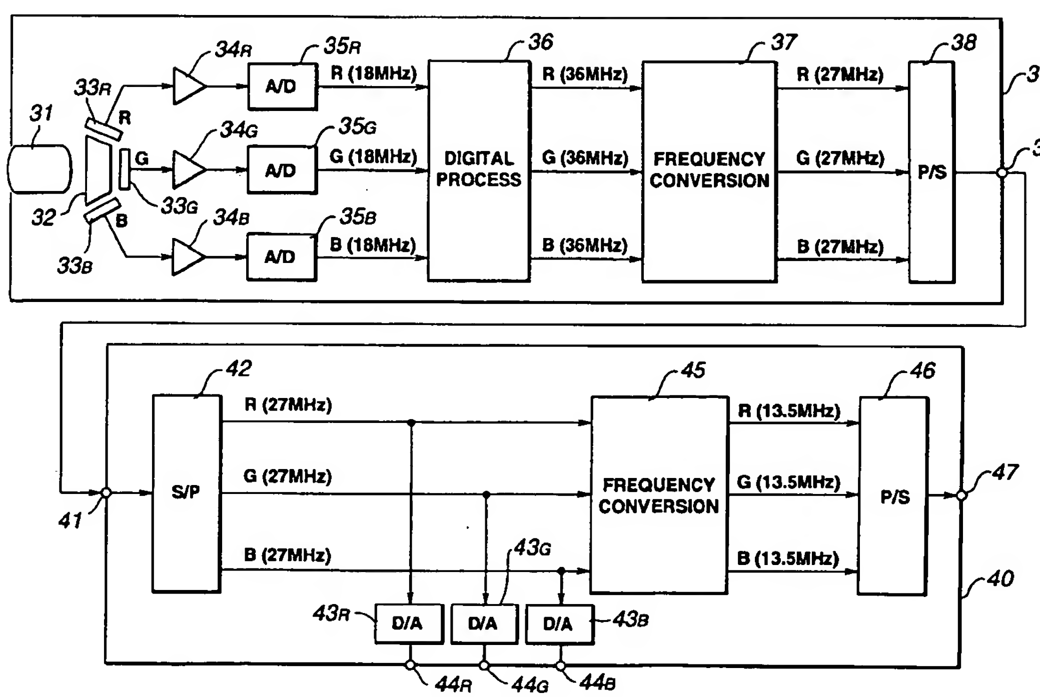
(57) **ABSTRACT**

A method and apparatus for transmitting digital color imaging signals to a camera controlling unit at a pre-set sampling rate obtained on imaging using a CCD imaging device. The sampling rate of at least one of plural signal components making up the digital color imaging signals is converted so that the sampling rate will be higher than the pre-set sampling rate. The digital color imaging signals containing at least one signal component having the converted sampling rate are transmitted to the camera control unit.

19 Claims, 7 Drawing Sheets



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